Exhibit 2

A simple Transputer-based CCD camera controller

N. R. Waltham

Rutherford Appleton Laboratory, Chilton,
Didcot, Oxon. OX11 0QX, UK

I. G. van Breda and G. M. Newton

Royal Greenwich Observatory, Herstmonceux Castle,
Hailsham, East Sussex, BN27 1RP, UK

ABSTRACT

This paper describes a CCD camera controller based on the Inmos Transputer chip, which is used for sequencing programmable waveform patterns, including windowed and pixel binning formats.

A key feature is the significant reduction in component count over previous systems made possible by the versatility and unique features of the Transputer. The outcome of this is that a complete controller for a single-chip CCD camera may be accommodated in a small enclosure on the cryostat used to cool the chip. Alternatively, extra drive cards may be added to the waveform sequencer to drive a multi-chip camera.

The use of the Transputer allows the controller to be incorporated naturally into a parallel processing system whereby several cameras can be operated within the telescope environment using simple serial control and data transfer links.

1. INTRODUCTION

Since CCDs were first applied in astronomy, a prime goal of system engineers has been to reduce the amount of electronics within the camera, without sacrificing its flexibility and programmability.

On the one hand there has been a desire to incorporate a high degree of programmability in order that the same electronics may be adapted to operate CCDs of differing format and from different manufactures. Many early systems were designed around bit-slice microprocessor technology with programmable microcode[1,2]. Although very flexible, these systems inevitably require many circuit boards. A typical configuration consists of a digital box containing the bit-slice processor, an analogue box containing the CCD clock drivers and signal processing electronics, and a preamplifier mounted on the side of the CCD dewar. Disadvantages of such systems are the separate chassis needed to house the electronics and their related power supplies, and the fact that the cabling interconnections are rather complex. Another concern is the inevitable problem of earthing and ground loops which can occur in this type of distributed arrangement.

Other groups have opted for simpler schemes ranging from hard-wired logic through semi-programmable systems employing EPROMs to store the CCD readout waveform patterns[3,4]. Other designs have used conventional microprocessors to provide programmability, but are still somewhat complex because of the speed of operation required[5].

With the advent of increasingly fast reduced instruction set and other types of microprocessor, however, it is now becoming feasible to construct very compact systems without sacrificing programmability. Leach[6] has recently described a system designed around a Motorola digital signal processing chip, in which the waveforms are stored within the internal memory of the processor and strobed out to the CCD drivers under program control.

A typical CCD camera requires several functions, in addition to waveform sequencing, to complete it, for example clock drivers, video amplification and signal processing, analogue-to-digital conversion, data transmission, and the more mundane, but equally important, functions such as chip temperature control and shutter operation.

Our goal has been to construct a complete CCD camera system contained within a compact box on the side of the CCD dewar, while minimising any sacrifice in programmability. The heart of the system is an Inmos T222 Transputer. It has recently come to our attention that the idea of using the Transputer as a digital waveform generator has also been investigated by Smith[7]. The architecture he has used differs in detail from the scheme described here which also includes the other functions needed for a complete camera system.

2. DESIGN ASPECTS

The design goals for our camera were:

(i) To contain all the camera electronics within a compact box on the side of the dewar, this in itself helping to reduce earthing and ground loop problems;

(ii) To support programmable waveform sequencing, thus enabling the user to modify the clocking sequences for operation of different CCD types;

(iii) To provide multiple window and on-chip pixel binning readout formats;

(iv) To keep down power dissipation as part of a general effort to reduce heating within the dome environment which prevents seeing degradation;

(v) To make the controller expandable to multi-chip operation.

We have aimed to make the camera easily adaptable to new ideas and circumstances. For example, the hardware has been made as simple and cheap as possible, so that if one card in the system needs to be replaced, to enable the use of a new type of solid state array, say, then it is practical and reasonable to exchange relevant parts of the system with new designs.

The Transputer was chosen as the central processor for several reasons:

(i) It is a powerful processor (10 MIPS for a 20MHz clock rate), with 4 Kbytes of on-chip RAM, and four high speed serial links (jumper selection for 5, 10 or 20 Mbits/sec);

(ii) It is exceptional in that it requires very little 'glue' logic to make a complete system;

(iii) It can boot from either an EPROM memory, or by down-loading a programme over any of the serial links. In 'boot-from-link' mode, the Transputer's simple protocol allows read and write access to its memory, thus greatly easing hardware debugging;

(iv) It uses CMOS, resulting in low power dissipation.

3. CAMERA HARDWARE

All the electronics associated with reading out a CCD, and digitising the data, are located within an enclosure small enough to be mounted on the side of the cryostat (Figure 1).

The electronics are divided into the following subsystems, each on its own printed circuit card:

(i) Transputer camera controller and waveform generator;

(ii) CCD clock driver and DC bias voltage supplies;

(iii) Video signal processor;

(iv) 'personality' card, responsible for camera house-keeping functions;

A power supply unit is also required for both logic and analogue circuitry.

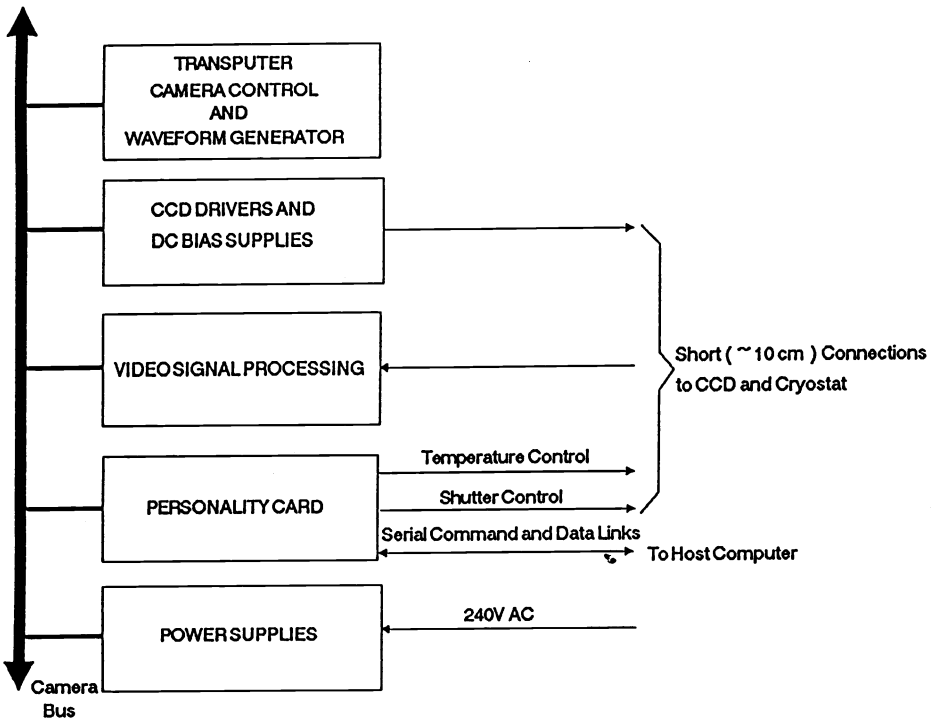

Figure 1. Schematic of camera controller.

Additional CCDs may be accommodated simply by adding additional CCD drive and video signal processing cards.

3.1. Sequencer

The components used in the sequencer card are shown in detail in Figure 2. A key feature is the small number of chips needed to build a complete sequencer.

The heart of the system is an Inmos T222 16-bit Transputer, whose main functions are:

(i) To receive and interpret command messages;

(ii) To generate all waveforms and sequences needed for CCD readout, including those needed for windowing, on-chip pixel binning and frame-transfer modes;

(iii) To send digitised image data down the camera data link;

(iv) To monitor camera status and operate the shutter, if fitted.

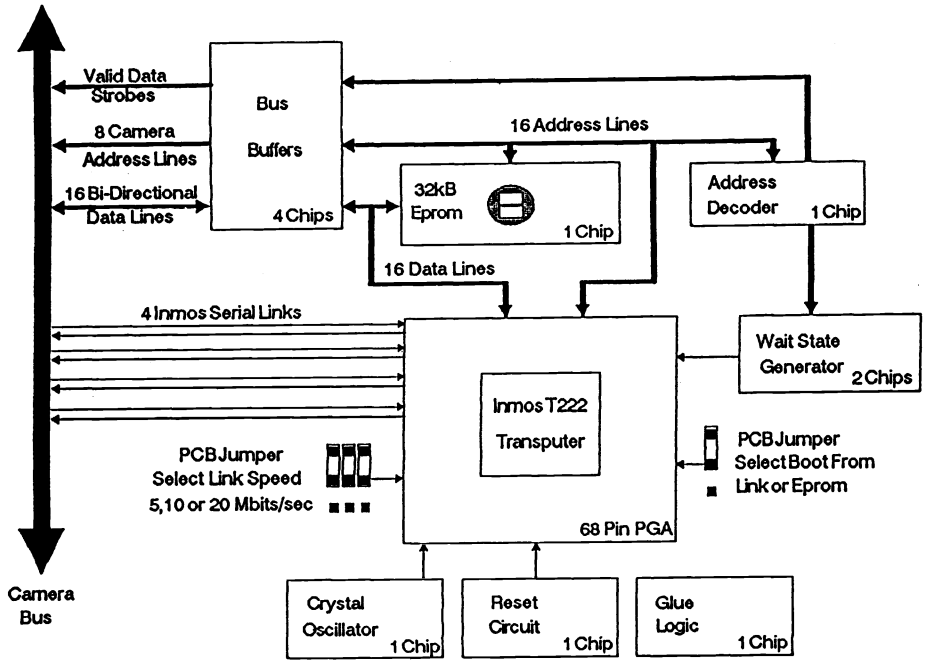

Figure 2. Sequencer card components.

The process of generating CCD readout waveforms consists of moving data from within a block of the Transputer's internal RAM memory to an external address decoded register; all the readout waveforms needed to operate the CCD are stored within roughly 2Kbytes of the T222's internal 4Kbyte memory.

The data transfer is done using the Transputer's block move instruction. This enables the user to specify source and destination addresses, and a byte count. When executed, the data is moved as 16-bit words from the source to the destination at a fixed rate determined by the number of 'wait states' programmed into the external access operation. A group of reserved destination addresses in the memory map is decoded to direct all the data to a single destination.

Each transfer operation takes a minimum of four cycles, one for the Transputer to fetch data from its internal memory, and three for it to write it out to the external register. Although the T222 is capable of two cycles external memory operation, we have added a programmable memory mapped wait state generator so that external peripheral circuitry can operate at its optimal rate, and this inserts a minimum of one wait state to each external memory access. Since a 20MHz processor is used, this means that the minimum duration for each waveform state is 200ns. This is a factor of two slower than can be achieved with bit-slice designs, but quite acceptable for our slow-scan camera systems. For those applications needing very slow readout, it is an easy matter to extend the basic 200nS cycle time up to 500nS, in 50nS increments, by adding further wait states via the programmable wait state generator circuitry.

The T222 16-bit processor has been chosen partly because it is able to operate from an 8-bit EPROM (the 32-bit devices require four), and partly to simplify the auxiliary circuitry and the printed circuit itself. This means that a certain degree of multiplexing is necessary in order to generate all the waveforms for driving a CCD and controlling the video signal processing and digitisation electronics. In practice, the multiplexing of the waveforms has not been found to impose any real constraints on overall waveform timing.

Apart from the 2K bytes of on-chip RAM used for clock waveforms, a further 1K is allocated to a readout format table. This table is basically a set of instructions that tell the Transputer which waveforms to generate next, and how many. It thus specifies the overall frame size, number of windows, and any pixel binning; it may be altered by the user in different readout situations. The remaining internal memory is used by software routines that must run rapidly during readout. For example, each pixel is handled by a block move instruction, as above, but the number of pixels in a line are counted in a conventional software loop that must be located in internal RAM to minimise overheads.

The overall camera control software is stored within the EPROM, together with default waveform patterns and CCD size. On power-up, the program automatically loads the defaults and transfers that part of the program which needs to run fast into the Transputer's memory. Less time critical operations such as the main camera command interpreter works from code within the EPROM.

Modifications to the waveform patterns and the readout table are possible by down-loading new data via the camera command link. The resident software then re-arranges the usage of the Transputer's internal memory accordingly.

The command and data links utilise the link hardware provided by the Transputer. The links can be configured using jumpers to select 5, 10 or 20 Mbits/sec data rates. Four such links are provided on the T222 Transputer. Thus, it is possible to have one link dedicated to camera command and status messages, a second to sending digitised CCD data, with two spare enabling communication with other peripherals such as a filter wheel, for example. During software development, one of the links may be connected to a host computer development system.

3.2. Clock drivers

The clock driver card translates the logic levels produced by the waveform sequencer into the high current drive analogue waveforms of appropriate amplitude and shape needed to drive the high capacitance electrodes on a CCD; it also includes the DC bias voltages needed to operate the chip.

The signal amplitudes need to be of the order of 10V and adjustable, with sloped rising and falling edges in the range 200 to 5000nS to facilitate charge transfer. An important aim has been to provide the necessary high-current drive without the high quiescent currents associated with high-speed circuitry.

CCDs sometimes require that the electrode phase used to collect charge during light integration be held at a lower voltage level during light integration than that applied during clocking[8]. This ability to have tri-level clock voltages can prove useful in overcoming luminescence defects found in some CCDs, and also for reducing dark current.

Two clock driver systems have been developed, one in which the various clock and DC bias voltage levels are set using potentiometers, and another in which they are set by digital-to-analogue converters.

The potentiometer board generates two groups of four-phase clock drivers, and a single reset clock driver phase, thus allowing operation of CCDs with up to four phases in full frame imaging mode. Seven DC bias voltages are also generated. One of these, the CCD output transistor drain supply, can be switched between two levels, which is sometimes useful in reducing output transistor diffusion luminescence in some CCDs.

The voltage levels for the clocks are generated from operational amplifiers feeding from a voltage reference (Figure 3). The clock pulses are derived from analogue switches connected to these voltage levels. Each clock signal uses an RC network to shape the waveform transitions. An Elantec EL2001 unity voltage gain, high current amplification buffer is used to drive the CCD electrodes. The EL2001 has the important virtue of a low quiescent current of 1.3 mA. Low noise operational amplifiers are used to supply the chip bias voltages.

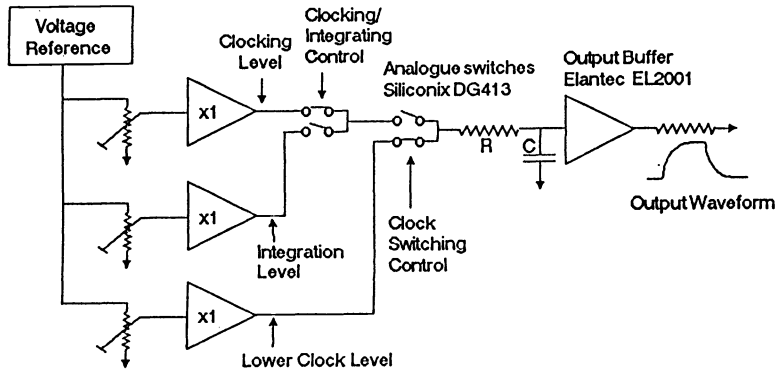

Figure 3. Potentiometer clock driver circuit.

RC shaping of the waveform before the output buffer has the advantage that the waveform can be set to the desired shape before it reaches the CCD. Waveform shape distortion due to capacitive loading from the CCD can thus be minimised, thus enabling the waveform phasing to be set without the CCD connected.

As indicated in Section 3.1, digital output from the sequencer must be multiplexed between the various clock signals. On this card, the clock lines are divided into banks of eight: the least significant bits of the sequencer output provide on/off bits for eight clock lines, the more significant select between two banks.

Each bank may be grouped according to function. For example, we have used bank 1 for the CCD imaging electrodes and bank 2 for the readout register electrodes. This card also allows four bits of the most significant byte to be used for a chip number, so chips within an array of up to 16 devices may either be driven collectively or as individuals. A PAL is used to decode bank selection and so a card's configuration can easily be modified by programming a new PAL.

Unfortunately, this type of clock driver requires a fair degree of printed circuit space to accommodate all the components, including the large number of potentiometers and decoupling capacitors. For these reasons, we have also constructed a card that uses digital-to-analogue converters to generate the CCD voltages. The availability of low power octal DAC chips has made such a scheme very attractive.

The DAC driver card has a similar specification to the potentiometer driver card, but has an additional set of four-phase drivers which allows independent clocking of the CCD imaging and storage areas. This means that a single card can operate a CCD in frame-transfer mode.

A typical clock driver is illustrated in Figure 4. An Analogue Devices AD7228 octal 8-bit DAC chip is used to generate the clock levels. This particular device does not produce sufficient output voltage swing in the desired range and so it is necessary to amplify and offset the output using a high-speed amplifier. The amplified waveform is passed through an RC filter and EL2001 buffer in a similar way to the potentiometer card.

Since the waveform levels are now set by data fed to the DACs, it becomes necessary to modify the sequencer waveforms and the associated multiplexing. The lower byte of each 16-bit data output from the sequencer is used to define the output voltage of an individual clock; the upper byte determines which DAC is to be modified.

The DC bias voltage DACs are addressed separately from those operated from the sequencer and use a separate area of the memory map, rather than operating directly from the sequencer output.

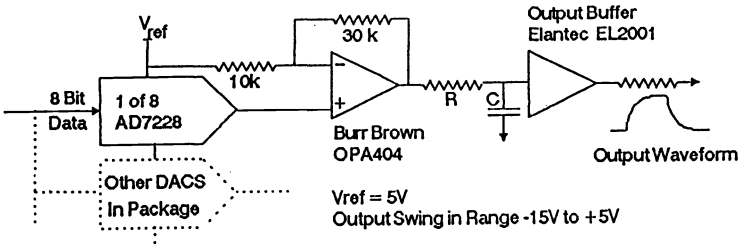

Figure 4. Digital-to-analogue converter clock circuit.

The multiplexing of the DACs means that only one clock output can be updated on any one sequencer output state transition, but this has not been found to impose any real constraints for slow-scanned CCD operation.

3.3. Signal processing

The circuitry on this card performs the preamplification of the CCD video signal, correlated double sampling signal processing to eliminate reset noise, and 16-bit digitisation.

There are basically two different correlated double sampling signal processing schemes: 'dual-slope integration', and a somewhat simpler approach known as 'clamp-and-sample'.

Initial work has been based on the clamp-and-sample method but we expect also to experiment with a variant of the dual-slope technique.

The analogue-to-digital converter is the Crystal CS5016. We chose this device for its performance, small size, low cost, and very low power dissipation.

Digitised video data are read into the Transputer at the end of each pixel cycle and immediately sent down a Transputer link.

For a multi-chip CCD camera, an additional video signal processing card and clock driver card need to be added for each additional CCD. This means that each CCD has its own ADC. This does not cause a problem due to the low cost and low power dissipation of the Crystal device. It has the distinct advantage that it is not necessary to consider multiplexing video waveforms from each CCD into the one ADC, a very difficult task to achieve if crosstalk between the various channels is to be kept below 16-bit digitisation levels.

3.4. Data link and house-keeping

The fourth card in the system is the 'personality' card, so called because it accommodates all those functions which make the camera specific to a particular application.

The principal functions are:

(i) CCD temperature control;

(ii) Shutter control;

(iii) Camera communication link buffers.

As an example, most astronomical imaging CCD cameras use a liquid nitrogen cooled cryostat to keep the chip cold, and thus minimise its dark current. These require a different form of temperature control from that used with, say, a Peltier-cooled autoguider CCD[9].

The same reasoning applies to camera shutter control: some cameras have their own shutter control circuitry, others may have their shutter built into the host instrument, but may require some form of synchronisation between CCD and host.

Camera communication link buffering can also be optimised for the operating environment: on the telescope, where the camera is usually remote from the main control centre, the use of fibre optic cabling offers advantages of high speed data transfer over long distances with complete electrical isolation. In the development laboratory, however, a cheaper system employing balanced RS422 twisted pair cabling could well be a more cost attractive solution.

All of the above can be accommodated by designing a specific personality card where the application demands it.

4. SOFTWARE

The CCD controller software was written in the Occam language, with the help of an IBM PC computer acting as host for an INMOS Transputer development system. Some time critical sections being written in assembler.

Occam models a software system as a number of 'processes' which communicate with each other via 'channels'. Channels may be either software channels (if the various processes are running on one Transputer), or 'hardware links' if the processes are running on more than one Transputer chip.

The CCD camera software consists of three modules (Figure 5), these being the command processor, the readout process, and the shutter control process. The readout and shutter control processes are invoked by the command processor; they are not executed in parallel.

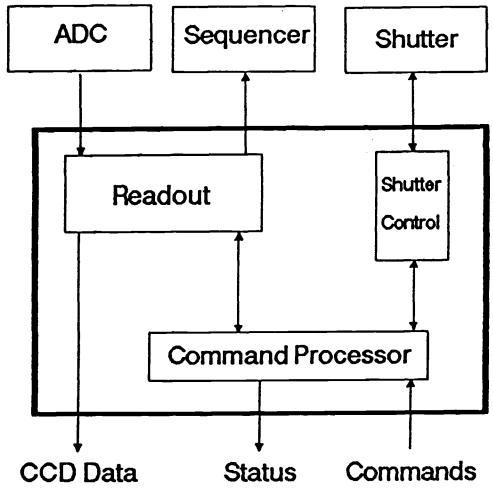

Figure 5. Software structure.

The command processor accepts commands from an Occam channel via one of the Transputer links. These include: setting of various parameters, such as CCD size, windowed readout format, binning factors and exposure time; compilation of the waveform readout table from the format parameters; shutter control; and readout execution.

The CCD controller commands take the form of a single character followed by a set of parameters unique to the command. For example, the command to set the overall frame size of the CCD readout consists of the ASCII character 'Z', followed by two binary encoded 16-bit integers denoting the x and y dimensions of the CCD. Each command returns a status byte plus optional data. The status byte informs the host computer of the result of the command. The use of a simple protocol enables drivers to be written in a variety of languages, and for a variety of machines and operating systems.

5. DATA ACQUISITION

Figure 6 shows the control and data acquisition system used for the development of the camera.

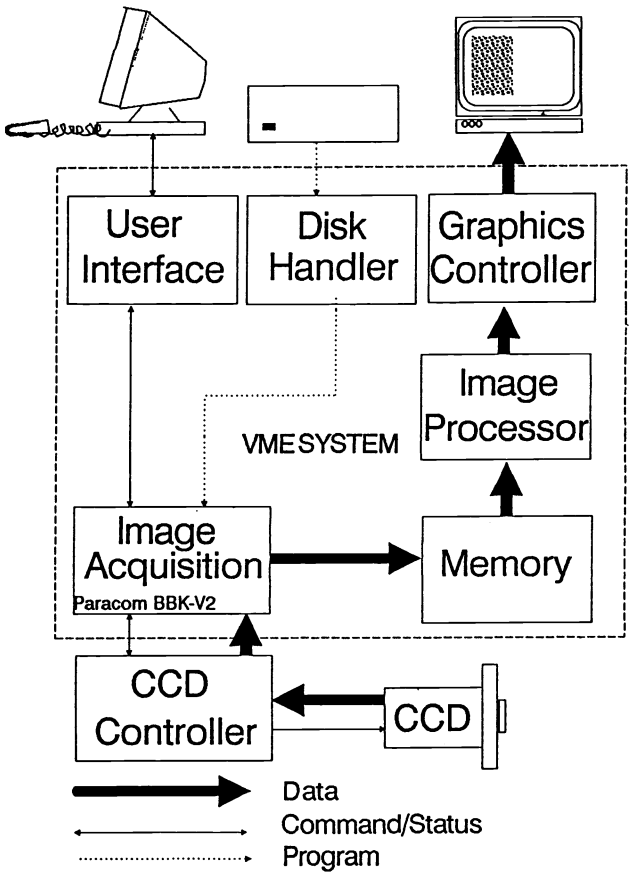

Figure 6. Data acquisition system.

The host computer system is built around a Motorola MC68020 processor running within a VME hardware environment. It is fitted with SCSI disks for programme and data storage, an image display card, and terminal interfaces. Image data from the detector are stored in a large 16 Mbyte RAM. The software running on the MC68020 is written in Forth.

A Paracom BBK-V2 VME Transputer card is used as the command and data acquisition interface between the imaging systems and the CCD camera. The Transputer on this card is booted by down-loading from the IBM PC based Transputer development system. Once running, commands may be sent via the VME bus and Transputer link to the CCD camera. The same link is used to receive CCD image data; the Transputer stores this data within VME memory, where it may be processed and displayed by the MC68020 processor.

In our laboratory arrangement, we have used the same link for both commands and data. At the telescope, however, where the control and data acquisition system is often tailored to the overall control of many instruments and detectors[10], there are strong arguments for separating the command and data channels, particularly in those systems which use a separate microprocessor system for acquiring and displaying detector data; the personality card may readily be arranged to handle this.

6. CONCLUSION

We have shown that the Transputer, as well as having the speed needed to generate CCD readout waveforms directly, also allows the electronics hardware to be greatly reduced compared with previous bit-slice and other camera systems.

We have aimed to make the camera modular and thus easily adaptable to new ideas and circumstances. Applications include both ground-based and space instrumentation: in particular, camera systems, attitude monitoring and guidance systems. It is equally applicable to optical CCDs and the newly emerging solid state infrared detectors.

The Transputer communications link enables the camera to be easily incorporated into a generalised parallel processing system where, for example, a second Transputer could be used for centroiding calculations in attitude monitoring and guidance systems.

7. REFERENCES

1. S. Marcus, R. Nelson and R. Lynds, "Preliminary evaluation of a Fairchild CCD-211 and a new camera system", Instrumentation in Astronomy III, Proc. SPIE, Vol. 172, pp. 207-231, 1979.

2. P. R. Jorden, D. J. Thorne and I.G. van Breda, "Royal Greenwich Observatory charge-coupled device camera", Instrumentation in Astronomy IV, Proc. SPIE, Vol. 331, pp. 87-95,1982.

3. J. E. Gunn and J. A. Westphal, "Care, feeding and use of charge-coupled device imagers at Palomar Observatory", Solid State Imagers for Astronomy, Proc. SPIE, Vol. 290, pp. 16-23, 1981.

4. E. D. Loh, "Princeton observing and picture-processing equipment", Solid State Imagers for Astronomy, Proc. SPIE, Vol. 290, pp. 150-154, 1981.

5. J. D. Bregman and N. R. Waltham, "Basic design of compact CCD controllers for the William Herschel Telescope", The Optimisation of the Use of CCD Detectors in Astronomy, Proc. ESO-OHP Workshop No. 25, pp. 127-136, 1986.

6. R. W. Leach, "Design of a CCD controller optimized for mosaics" Pub. A.S.P. Vol 100, Oct 1988, pp. 1287-1295.

7. R. M. Smith, "Programmable digital waveform generator", Microprocessors and Microsystems Vol 13, No. 3, April 1989, pp. 149-159.

8. D. J. Thorne, P. R. Jorden and N. R. Waltham, "Optimisation of CCDs for astronomy - the RGO experience", The Optimization of the Use of CCD Detectors in Astronomy, Proc. ESO-OHP Workshop No. 25, pp. 13-37,1986.

9. D. J. Thorne, N. R. Waltham, G. M. Newton, I. G. van Breda, M. Fisher, "The CCD guidance sensors for the William Herschel Telescope", Instrumentation in Astronomy VII, Proc. SPIE, Vol. 1235 (these proceedings), 1990.

10. I. G. van Breda, G. M. Newton, A. N. Johnston, N. R. Waltham, "Use of Transputers in instrument control systems", Instrumentation in Astronomy VII, Proc. SPIE, Vol. 1235 (these proceedings), 1990.